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L1	2	((("5678567") or ("5771370"))).PN.	USPAT	OR	OFF	2005/07/19 13:36
L2	35	optimize and hardware and software and co-simulation	USPAT	OR	OFF	2005/07/19 13:34
L3	37	optimize and hardware and software and co-simulation	USPAT	OR	ON	2005/07/19 13:34
L4	2	((("5768567") or ("5771370"))).PN.	USPAT	OR	OFF	2005/07/19 13:37
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L8	0	"09586433"	US-PGPUB	OR	OFF	2005/07/19 13:39
L9	0	"09/586,433"	US-PGPUB	OR	OFF	2005/07/19 13:39
L10	1	bortfeld.in.	US-PGPUB	OR	OFF	2005/07/19 13:43
L11	1	("6718294").PN.	USPAT	OR	OFF	2005/07/19 13:45
L12	1	(memory adj3 model) and (processor adj3 model) and software and (single adj3 (process or thread)) and (cycle adj3 accurate) and (function adj3 call)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/19 14:15
L13	1	"772140"	EPO	OR	ON	2005/07/19 14:17
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25. A demonstration of co-design and co-verification in a synchronous language

Singh, S.;

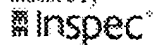
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Christoph Kern, Mark R. Greenstreet

April 1999 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**,

Volume 4 Issue 2

Full text available: [pdf\(411.53 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In recent years, formal methods have emerged as an alternative approach to ensuring the quality and correctness of hardware designs, overcoming some of the limitations of traditional validation techniques such as simulation and testing. There are two main aspects to the application of formal methods in a design process: the formal framework used to specify desired properties of a design and the verification techniques and tools used to reason about the relationship between a spec ...

Keywords: case studies, formal methods, formal verification, hardware verification, language containment, model checking, survey, theorem proving

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January 1980 **ACM SIGACT News**, Volume 12 Issue 1

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3 [High-level design verification of microprocessors via error modeling](#)

D. Van Campenhout, H. Al-Asaad, J. P. Hayes, T. Mudge, R. B. Brown

October 1998 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**,

Volume 3 Issue 4

Full text available: [pdf\(174.30 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

A design verification methodology for microprocessor hardware based on modeling design errors and generating simulation vectors for the modeled errors via physical fault testing techniques is presented. We have systematically collected design error data from a number of microprocessor design projects. The error data is used to derive error models suitable for design verification testing. A class of basic error models is identified and shown to yield tests that provide good coverage of comm ...

Keywords: design errors, design verification, error modeling

4 A Multi-Level Transformation Approach to HW/SW Codesign: A Case Study

Tommy King-Yin Cheung, Graham Hellestrand, Prasert Kanthamanon

March 1996 **Proceedings of the 4th International Workshop on Hardware/Software Co-Design**

Full text available:  pdf(970.93 KB)

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This reported work applies a transformational synthesis approach to hardware/software codesign. In this approach, the process of algorithm design is coupled early on with hardware design to allow for a complete design space exploration. Both the specification and the transformation mechanisms are encoded in a functional notation, called form, which facilitates algorithmic derivation, structural transformation and verification. In the algorithmic derivation phase, possible computational schedules ...

Keywords: Functional Languages, Design Transformations.

5 An architecture design and assessment system for software/hardware codesign

Connie U. Smith, Geoffrey A. Frank, John L. Cuadrado

June 1985 **Proceedings of the 22nd ACM/IEEE conference on Design automation**

Full text available:  pdf(908.59 KB)

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Codesign of hardware and software for high performance signal processing systems is important if the potential benefits of VLSI are to be realized. This article describes a CAD system developed to support the codesign of hardware and software architectures for high performance digital signal processors which is based on a directed graph methodology. A comprehensive example is developed to demonstrate the use of the system, the fundamentals of the modeling and analysis methodology are discussed ...

6 High-level scheduling model and control synthesis for a broad range of design applications

Chih-Tung Chen, Kayhan Küçükçakar

November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design**

Full text available:  pdf(110.32 KB)

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This paper presents a versatile scheduling model and an efficient control synthesis methodology which enables architectural (high-level) design/synthesis systems to seamlessly support a broad range of architectural design applications from datapath-dominated digital signal processing (DSP) to micro-processors/controllers and control-dominated peripherals, utilizing multi-phase clocking schemes, multiple threading, data-dependent delays, pipelining, and combinations of the above. The work presented ...

Keywords: control synthesis, scheduling model, multi-phase clocking, multi-threading, pipelining, relative scheduling, high-level synthesis, architectural synthesis, behavioral synthesis, architectural power optimization.

7 High-level synthesis and codesign methods: an application to a videophone codec

Pierre Paulin, Jean Fréhel, Michel Harnand, Elisabeth Berrebi, Clifford Liem, François Naçabal, Jean-Claude Herluison

December 1995 **Proceedings of the conference on European design automation**

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8 Enhancing simulation with BDDs and ATPG

Malay K. Ganai, Adnan Aziz, Andreas Kuehlmann

June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**



Full text available:  [pdf\(795.60 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

Keywords: ATPG, BDDs, coverage, formal verification, simulation

9 Standards for system-level design: practical reality or solution in search of a question?

Christopher K. Lennard, Patrick Schaumont, Gjalt de Jong, Anssi Haverinen, Pete Hardee

January 2000 **Proceedings of the conference on Design, automation and test in Europe**

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